(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 November 2001 (29.11.2001)

PCT

(10) International Publication Number
WO 01/91095 A1

(51) International Patent Classification[7]: G09G 3/32

(21) International Application Number: PCT/EP01/04674

(22) International Filing Date: 25 April 2001 (25.04.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
00201801.8 22 May 2000 (22.05.2000) EP

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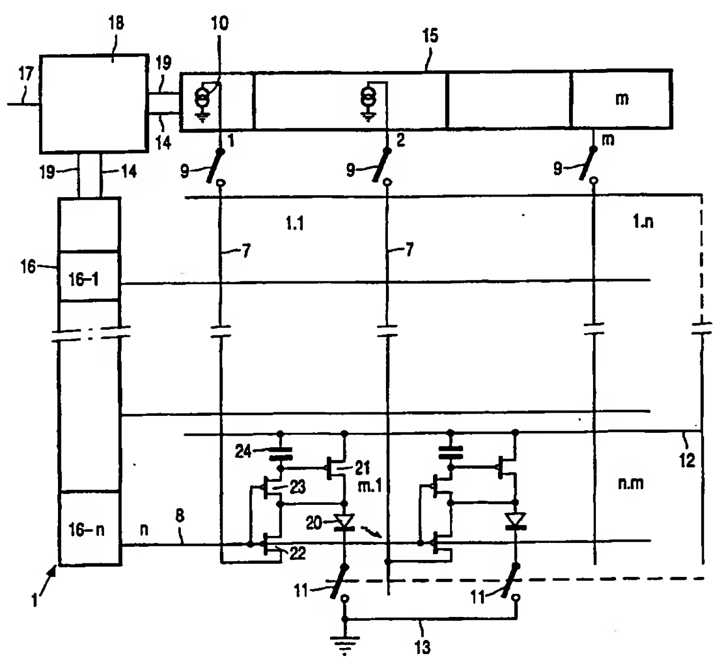
(81) Designated States (*national*): CN, JP, KR.

(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY DEVICE



(57) Abstract: Grey scale linearity and power efficiency in active matrix (O) LEDs are enhanced by storing the grey value in a memory circuit, coupled to an adjusting circuit, preferably via a current mirror.

WO 01/91095 A1

ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY DEVICE

The invention relates to a display device comprising a matrix of pixels at the area of crossings of row and column electrodes, each pixel comprising at least a current adjusting circuit based on a memory element, in series with a luminescent element.

Such electroluminescence-based display devices are increasingly based on (polymer) semiconducting organic materials. The display devices may either luminesce via segmented pixels (or fixed patterns) but also display by means of a matrix pattern is possible. The adjustment of the pixels via the memory element determines the intensity of the light to be emitted by the pixels. Said adjustment by means of a memory element, in which extra switching elements are used (so-called active drive) finds an increasingly wider application.

Suitable fields of application of the display devices are, for example, mobile telephones, organizers, etc.

A display device of the type described in the opening paragraph is described in PCT WO 99/42983. In said document, the current through a LED is adjusted by means of two TFT transistors per pixel in a matrix of luminescent pixels; to this end, a charge is produced across a capacitor via one of the TFT transistors. This TFT transistor and the capacitor constitute a memory element. After the first TFT transistor has been turned off, the charge of the capacitor determines the current through the second TFT transistor and hence the current through the LED. At a subsequent selection, this is repeated.

In this drive mode, the charge across the capacitor is adjusted in such a way that the LED is switched between two modi, namely the "high power mode" and the "low power mode", in which the mutual time ratio between the two modi determines the grey value. To adjust this mutual ratio accurately, many extra electronics are required, inter alia, a processor and converters. Moreover, dependent on the grey value, switching between the two modi must be effected at high frequencies. This leads to an increased power consumption and hence faster ageing. Moreover, artefacts occur in moving images.

It is, inter alia, an object of the present invention to provide a display device of the type described in the opening paragraph in which the above-mentioned problems occur to a lesser extent. To this end, such a display device is characterized in that the device comprises means at the area of a pixel for adjusting a current through the luminescent element, as well as a switch between a plurality of luminescent elements and a connection point for an operating voltage.

By means of the switch (for example, a TFT transistor or a bipolar transistor), the luminescent elements are provided with a current corresponding to the desired luminance. During adjustment of a part of the drive circuit, the switch may be closed, if desired. However, it is opened during a part of a frame period. Parts of this drive circuit (for example, the combination of a capacitor and a transistor) determine the ultimate current through the luminescent elements. Since the luminescent elements can now convey current for a much shorter time, they are preferably driven in the so-called constant efficiency range. Here, the efficiency of the LED as a function of the diode voltage is practically constant. With a shorter time of conveying current through the LED (on-time), the current at a given luminance is usually so high that the LED is driven in this constant efficiency range.

In a first embodiment, the means for adjusting a current through the luminescent element comprise at least one switching element between a column electrode and a connection point of the memory element.

A preferred embodiment of a display device according to the invention is characterized in that the column electrode can be electrically coupled to a current source, and in that such a further circuit is arranged between the column electrode and the connection point of the memory element that the current adjusting circuit substantially does not conduct during adjustment of the value of the current through the luminescent element. This limits the dissipation.

The further circuit is preferably electrically detachable from the adjusting switch, while a transistor of this further circuit, together with a transistor in the memory element in the coupled state, constitutes a current mirror. Notably when all switches are made in one process (for example, TFTs in polysilicon technology) this results in uniform properties (and thus adjustments) of the switches throughout the display surface area.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows diagrammatically a display device according to the invention,

Fig. 2 shows the efficiency and the current through a LED as a function of the voltage,

Fig. 3 shows transistor characteristics of transistors used in Fig. 1, while

Fig. 4 shows an associated time diagram, and

Fig. 5 diagrammatically shows a further pixel according to the invention.

The Figures are diagrammatic; corresponding components are generally denoted by the same reference numerals.

Fig. 1 shows diagrammatically an equivalent circuit diagram of a part of a display device 1 according to the invention. This display device comprises a matrix of (P) LEDs or (O) LEDs 14 with n rows (1, 2, ..., n) and m columns (1, 2, ..., m). Where rows and columns are mentioned, they may be interchanged, if desired. This device further comprises a row selection circuit 16 and a data register 15. Externally presented information 17, for example, a video signal, is processed in a processing unit 18 which, dependent on the information to be displayed, charges the separate parts 15-1, ..., 15-n of the data register 15 via supply lines 19.

The selection of a row takes place by means of the row selection circuit 16 via the lines 8, in this example, gate electrodes of TFT transistors or MOS transistors 22, by providing them with the required selection voltage.

Writing data takes place in that, during selection, the current source 10, which may be considered to be an ideal current source, is switched on by means of the data register 15, for example, via switches 9. The value of the current is determined by the contents of the data register. The current source 10 may be common for a plurality of rows. If this is not the case, the switches 9 may be dispensed with. Where this application states the phrase "can be electrically coupled to the current source", this case is also considered to be included.

During addressings, the capacitor 24 is provided with a certain charge via the transistors 21, 22 and 23. This capacitor determines the adjustment of the transistor 21 and hence the actual current through the LED 20 during the drive period, and the luminance of (in this example) the pixel (n,1), as will be described hereinafter. Mutual synchronization between the selection of the rows 8 and the presentation of voltages to the columns 7 takes place by means of the drive unit 18 via drive lines 14.

At the instant when a row, in this example row 1, is selected, the current source 10 starts to convey current. During selection, information is presented from column register 15 (in this example) via the line 7. This information determines the current through the (adjusting) transistors 21, 22 and 23 so that the capacitor 24 acquires a given charge, dependent on the conveyed current and the period of time. The other plate of the capacitor 24 is connected to the positive power supply line 12. After selection (after closure of the switch 9), this capacitor has a certain charge which determines the voltage at the gate of (control) transistor 21. The capacitor and the (control) transistor 21 jointly constitute the memory element mentioned above. The diodes (LED) 20 conduct in dependence upon the adjustment of this transistor 21. According to the invention, this conductance is regularly interrupted whereafter a new value of this conductance is adjusted or not adjusted and restored after one or more rows of pixels have been adjusted, i.e. when all transistors 21 in a number of rows have been adjusted in the manner described. At that instant (and preferably at the end of a frame time), a common switch 11 is closed for a short time so that current can flow through the transistors 21 and the LEDs 20 so that the LEDs luminesce in conformity with the adjusted value.

The advantage thereof will be described with reference to Fig. 2. This Figure shows, as a function of the voltages across a LED, the (logarithm of the) efficiency (solid line) of the LED and the current (broken line) through the LED. The Figure shows that this efficiency reaches a given maximum from a voltage V_1. The current through the LEDs (and hence the luminance) increases substantially exponentially from V_1. Since the switches 11 between one or more LEDs 20 and, for example, ground (in this example via the line 13) are not closed during the entire frame time, the LEDs convey current for a shorter time so that the desired quantity of light can be emitted with a higher efficiency and a shorter current pulse. The switches 11 may also be closed after a part of the lines (1/2, ¼, ...) has been written (referred to as sub-frame driving).

The adjustable currents preferably have such values that they are practically always larger than the current I_1 (Fig. 2) associated with the voltage V_1. To this end, the transistor 21 has a characteristic as is shown in Fig. 3. In this embodiment, transistor 21 is a TFT transistor of the p type which, dependent on the gate voltages V_{g1}-V_{g4} supplies currents between I_2 and I_3 (Fig. 3), which currents are larger than I_2, while the range I_2-I_3 is sufficiently wide to adjust all grey values in the high efficiency range.

The operation of the display device is explained once more with reference to Figs. 1 and 4. By switching on current sources 10 associated with columns 1 to m (Fig. 4(d))

during consecutive selection of the rows 1 to n (Figs. 4(a), 4(b), 4(c)), a capacitor 24 is provided with a certain charge in each of the pixels. The information as stored in data register 15 determines, in a way similar to that described above for transistor 21, the current through transistors 22 and 23. The voltage on the supply line 12 is such that one plate of the capacitor and hence node 25 receives a voltage in the range V_{g1}-V_{g4}, which voltage is maintained after the current source 10 has been switched off.

The voltage at the node 25 and hence the voltage at the gate of transistor 21 is in the range V_{g1}-V_{g4}. However, the transistor 21 cannot conduct if the switch 11 is opened. This switch is not closed in this example until after the end of the frame period t_F after the period t_{charge} in which all pixels are charged. The switch 11 is closed, for example, for a short period t_{switch}, which period is long enough to cause the associated diodes (LED) 20 to luminesce in the correct adjustment. Since all (desired) LEDs are on for a short time with a maximal efficiency, there is less degradation in this drive mode than in the customary passive and active structures. By means of a drive circuit (not shown) the duty cycle $\frac{t_{switch}}{t_f}$ of the switch is adjusted, if desired, as a function of temperature or ageing, such that the efficiency remains substantially constant (optimal). It is also possible to choose the duty cycle to be different per color (in a color display device) and thus to obtain an optimal color point.

The switch 11 is preferably realized in monocrystalline silicon. In this way, a large current required for driving the total number of pixels can be supplied rapidly. This switch may be realized, for example, in a drive IC. Use may also be made of some parallel switches.

In the circuit of Fig. 1, one of the (adjusting) transistors 22, 23 may be dispensed with, if necessary. A variant is shown in Fig. 5 with an extra transistor 26 which is substantially identical to transistor 22 and has a gate which is connected via a switch 27 to the node 25 and hence to the gate of transistor 21, the gate width of which is, for example, ten times that of transistor 26. During charging of the capacitor 24, switch 27 is closed so that the voltage at node 25 acquires the desired value. At the end of the selection time, or at another suitable instant, switch 27 is opened. The voltage across the capacitor again determines the current through transistor 21 and hence the current through the LED 20 during the period when switch 11 is closed. The voltage at the memory element comprising the capacitor 24 and transistor 21 can now be adjusted by means of the "current mirror" constituted by the transistors 26, 27 with a much smaller current (a factor of 10 smaller) than that at which the

LED is operated. After adjustment of a number or of all pixels, a plurality of LEDs 20 is driven simultaneously by closing one or more switches 11.

Several variations are of course possible within the scope of the invention. In given applications, not all pixels need to be adjusted in advance before the LED drive is started. A realization with bipolar transistors is also feasible.

The protective scope of the invention is not limited to the embodiments described. The invention resides in each and every novel characteristic feature and each and every combination of features. Reference numerals in the claims do not limit the protective scope of these claims. The use of the verb "to comprise" and its conjugations does not exclude the presence of elements other than those stated in the claims. The use of the article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements.

CLAIMS:

1. A display device comprising a matrix of pixels at the area of crossings of row and column electrodes, each pixel comprising at least a current adjusting circuit based on a memory element, in series with a luminescent element, characterized in that the display device comprises means at the area of a pixel for adjusting a current through the luminescent element, as well as a switch between a plurality of luminescent elements and a connection point for an operating voltage.

2. A display device as claimed in claim 1, characterized in that the means for adjusting a current through the luminescent element comprise at least one switching element between a column electrode and a connection point of the memory element.

3. A display device as claimed in claim 1, characterized in that the column electrode can be electrically coupled to a current source, and in that such a further circuit is arranged between the column electrode and the connection point of the memory element that the current adjusting circuit substantially does not conduct during adjustment of the value of the current through the luminescent element.

4. A display device as claimed in claim 3, characterized in that the memory element comprises a TFT transistor and a capacitor between the gate electrode and a further connection of the TFT transistor, and in that the further circuit comprises at least one TFT transistor with a gate electrode connected to a row electrode.

5. A display device as claimed in claim 4, characterized in that the further circuit comprises two series-arranged TFT transistors between the column electrode and the memory element, which transistors have their gate electrodes connected a common row electrode, the common point of the two series-arranged TFT transistors being connected in an electrically conducting manner to an electrode of the luminescent element.

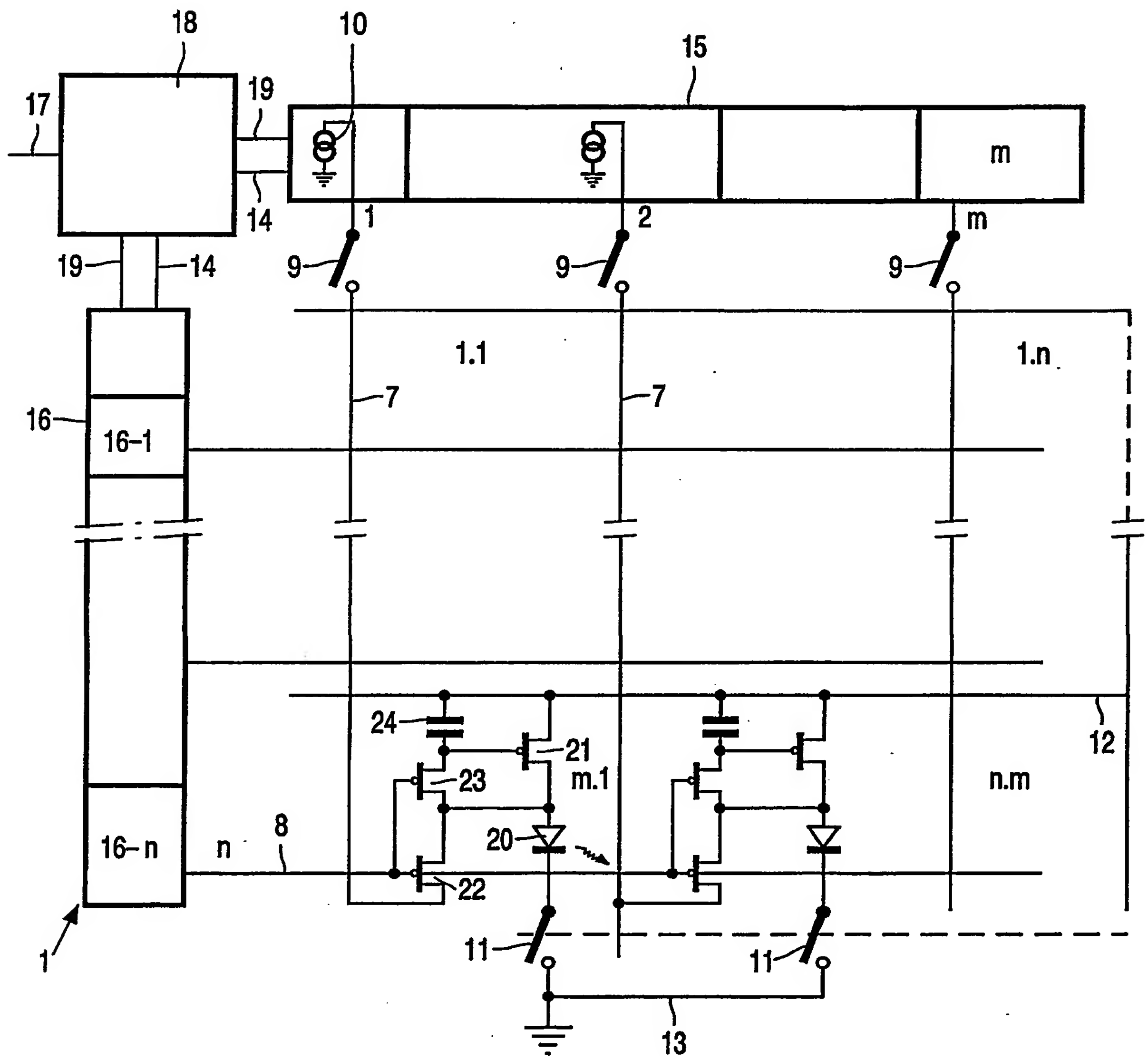
6. A display device as claimed in claim 3, characterized in that the further switch is electrically detachable from the memory element, and in that, in the coupled state, the further circuit constitutes a current mirror with the memory element.

7. A display device as claimed in claim 5, characterized in that the current mirror is asymmetrical.

8. A display device as claimed in claim 1, characterized in that said display device comprises drive means for varying the time during which the switch is closed.

9. A color display device as claimed in claim 8, characterized in that the drive means for luminescent elements of a different color can close associated switches during different periods of time.

10. A display device as claimed in claim 1, characterized in that the luminescent element comprises an organic LED or a polymer LED.



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n
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13

FIG. 1

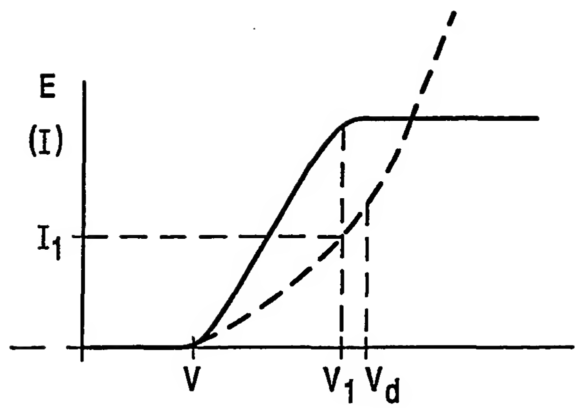

FIG. 2

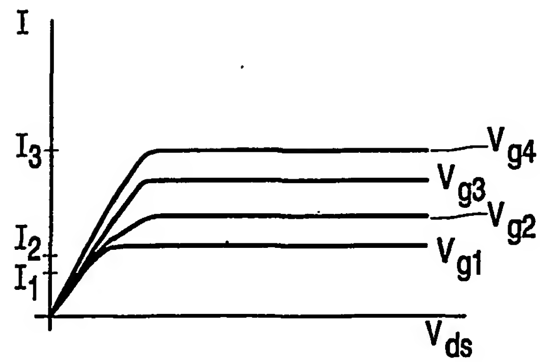

FIG. 3

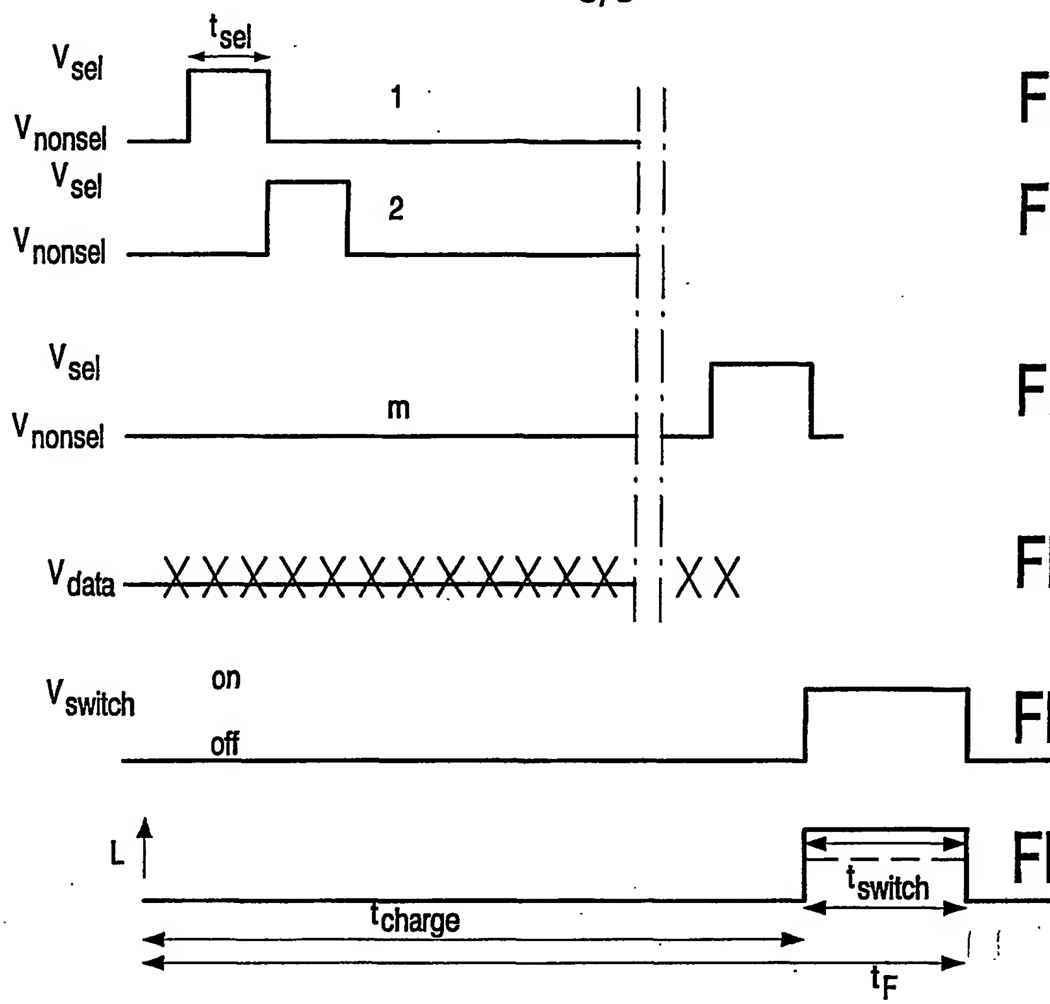

FIG. 4a

FIG. 4b

FIG. 4c

FIG. 4d

FIG. 4e

FIG. 4f

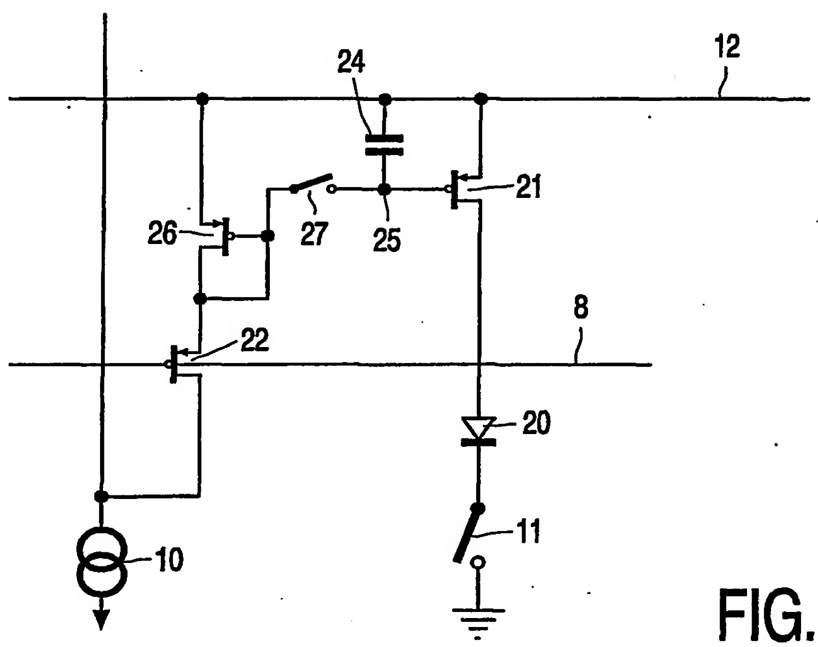

FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 01/04674

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 990 629 A (SHIOYA MASAHARU ET AL) 23 November 1999 (1999-11-23) abstract; figures 1,8,12,14-16,19,23,27-30 column 5, line 47 -column 7, line 7	1-4,6-8, 10
A	column 22, line 50 -column 28, line 5 column 39, line 21 -column 40, line 40	9
Y	WO 99 65012 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS SVENSKA AB (SE)) 16 December 1999 (1999-12-16)	1-4,6-8, 10
A	abstract; figures 2,3 page 8, line 6 -page 9, line 27 page 10, line 7 -page 11, line 6	5

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
28 September 2001	08/10/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Van Roost, L

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 01/04674

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